In the Claims:

1. (currently amended) A method for reducing power utilized by a

processor comprising the steps of:

determining that a processor is transitioning from a computing mode

to a mode in which a system clock to the processor is disabled, and

reducing core voltage to the processor to a value sufficient to maintain

state during the mode in which said system clock is disabled, wherein said

value of the core voltage is not sufficient to maintain processing activity in

said processor,

responsive to said determining, at a voltage regulator supplying said

core voltage, transitioning from a first regulation mode to a second regulation

mode,

wherein power is dissipated during a voltage transition that reduces

said selectable voltage in said first regulation mode and power is saved

during said voltage transition in said second regulation mode.

2. (currently amended) The [[A]] method as claimed in Claim 1 in which

the step of determining that a processor is transitioning from a computing

mode to a mode in which system clock to the processor is disabled comprises

monitoring a stop clock signal.

TRAN-P059/ACM/NAO Examiner: Cao, C.

Serial No.: 09/694,433 Group Art Unit: 2115

- 3. (currently amended) The [[A]] method as claimed in Claim 1 in which the step of reducing core voltage to the processor to a value sufficient to maintain state during the state in which system clock is disabled comprises furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor.
- 4. (Previously Presented) A method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled, and

reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled by:

furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor, and providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage.

5. (currently amended) A method for reducing power utilized by a system having a least a processor, comprising the steps of:

determining that [[a]] the processor is transitioning from a computing mode to a mode in which \underline{a} system clock to the processor is disabled,

TRAN-P059/ACM/NAO Examiner: Cao, C.

Serial No.: 09/694,433 Group Art Unit: 2115 reducing core voltage <u>being furnished by a voltage regulator</u> to the processor to a value sufficient to maintain state during the mode in which <u>the</u>

system clock is disabled, and

transferring operation of [[a]] the voltage regulator furnishing core

voltage in a mode in which power is dissipated during a voltage transition in

reduction[[s]] in core voltage to a mode in which power is saved during [[a]]

said voltage transition in the reduction in core voltage when it is determined

that [[a]] the processor is transitioning from [[a]] the computing mode to [[a]]

the mode [[is]] in which the system clock to the processor is disabled.

6. (currently amended) The [[A]] method as claimed in Claim 5 further

comprising the steps of returning the voltage regulator to its original mode of

operation when the value of the core voltage sufficient to maintain state

during the mode in which system clock is disabled is reached.

7. (currently amended) A circuit for providing a regulated voltage to a

processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the

selectable voltage level;

TRAN-P059/ACM/NAO Examiner: Cao, C.

Serial No.: 09/694,433 Group Art Unit: 2115

means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode, wherein the level less than that for operating the processor

means for changing the voltage regulator from a mode in which power is dissipated during a voltage transition that reduces said selectable voltage to a mode in which power is saved during said voltage transition.

in a computing mode is sufficient to maintain state of the processor; and

- (Original) A circuit as claimed in Claim 7 in which the means for providing signals at the input terminal of the voltage regulator comprises means for accepting binary signals indicating different levels of voltage.
- (currently amended) The [[A]] circuit as claimed in Claim 7 in which 9. the means for providing signals at the input terminal of the voltage regulator comprises:

selection circuitry,

means for furnishing a plurality of signals at the input to the selection circuitry, and

means for controlling the selection by the selection circuitry.

10. (currently amended) The [[A]] circuit as claimed in Claim 9 in which: the selection circuitry is a multiplexor, and

> Serial No.: 09/694,433 Group Art Unit: 2115

TRAN-P059/ACM/NAO Examiner: Cao, C.

the means for controlling the selection by the selection circuitry

includes a control terminal for receiving signals indicating a system

clock to the processor is being terminated.

11. (previously presented) A circuit for providing a regulated voltage to a

processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable

voltage level;

means for providing signals at the input terminal of the voltage

regulator for selecting a voltage for operating the processor in a

computing mode and a voltage of a level less than that for

operating the processor in a computing mode; and

means for reducing the selectable voltage below a lowest level the

voltage regulator is specified to output.

12. (Previously Presented) A circuit for providing a regulated voltage to a

processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage;

an input terminal for receiving signals indicating the selectable

voltage level; and

a voltage regulator feedback circuit;

means for providing signals at the input terminal of the voltage

regulator for selecting a voltage for operating the processor in a

computing mode and a voltage of a level less than that for operating

the processor in a computing mode; and

means for reducing the selectable voltage below a level provided

by the voltage regulator comprising:

a voltage divider network joined between the output

terminal and a voltage source furnishing a value higher than

the selectable voltage, and

the voltage regulator feedback circuit receiving a value

from the voltage divider network.

13. (currently amended) A circuit for providing a regulated voltage to a

processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable

voltage level;

means for providing signals at the input terminal of the voltage

regulator for selecting a voltage for operating the processor in a computing

mode and a voltage of a level less than that for operating the processor in a

computing mode;

circuitry for conserving charge stored by the voltage regulator when

the selectable voltage decreases changing the voltage regulator from a mode

in which power is dissipated during a voltage transition in reduction of the

selectable voltage to a mode in which system power is saved during said

voltage transition in reduction of the selectable voltage, and

means for enabling the circuitry for conserving charge stored by the

voltage regulator when the selectable voltage decreases.

14. (Previously Presented) A circuit for providing a regulated voltage to a

processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

TRAN-P059/ACM/NAO Examiner: Cao, C.

Serial No.: 09/694,433 Group Art Unit: 2115

an input terminal for receiving signals indicating the selectable

voltage level; and

a voltage regulator feedback circuit;

circuitry coupled to said input terminal and configured to provide

signals to the input terminal for selecting a first voltage for operating the

processor in a first mode and a second voltage for operating the processor in a

second mode;

a voltage source furnishing a value higher than the selectable voltage;

and

a feedback circuit coupled to the voltage source, the output terminal,

and the voltage regulator feedback circuit.

15. (Previously Presented) The circuit of Claim 14, wherein the first

voltage is for operating the processor in a computing mode and the second

voltage is a level less than that for operating the processor in the computing

mode.

16. (Previously Presented) The circuit of Claim 15, wherein the feedback

circuit comprises a voltage divider.

TRAN-P059/ACM/NAO Examiner: Cao, C.

Serial No.: 09/694,433 Group Art Unit: 2115

17. (Previously Presented) The circuit of Claim 14, wherein the feedback

circuit comprises a voltage divider.

18. (Previously Presented) The method of Claim 4, wherein the output

voltage to which said voltage regulator is reduced depends upon output

voltage of said voltage regulator prior to furnishing the input to reduce the

output voltage provided by the voltage regulator.

19-37 (canceled) (election)

TRAN-P059/ACM/NAO Examiner: Cao, C.

Serial No.: 09/694,433 Group Art Unit: 2115